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The Performance Analysis, Mathematical Modeling and Simulation Of pHEMT Based Transistor

[1] Tejal Rupwate, [2] Kishor G. Sawarkar

[1] ME student at MCT's RGIT,Mumbai, [2] MCT's RGIT,Mumbai.

Abstract: - **This article presents performance analysis and mathematical modeling of pHEMT based transistor from FET family utilizing AWR microwave office tool. In this work the performance of pHEMT based transistor (proposed model) on the basis of Gain, Noise Figure, S-parameter and Stability is compared with conventional transistor model without lumped elements at high frequency. By differing outside components of a proposed transistor without changing its proportional circuit components, improved transistor model has designed which has better circuit estimations at microwave range. The pHEMT based transistors have numerous applications in different microwave spaces, such as wideband radio astronomy application, Square kilo meter array (SKA) application, cryogenic broadband ultra-low noise MMIC applications, Low noise amplifier, RADAR and many more applications.**

Keywords: - **Pseudomorphic High Electron Mobility Transistor (pHEMT), Advancing the Wireless Revolution (AWR), Monolithic Microwave Integrated Circuit (MMIC).**

I. INTRODUCTION

Device modeling is an important aspect of circuit simulation. The most common way in modeling FETs is the use of an equivalent circuit. With the demands for higher performance, rapid prototyping, as well as lower cost for such systems and circuits, computer aided design (CAD) and simulation tools together with models for circuit elements have become increasingly important. To predict intermodulation, output power and efficiency etc., with high accuracy, a good nonlinear model for the transistor is required. The aim of this paper is to build a small signal model for high frequency microwave applications, where transistors are excited with varying terminal voltages. If the excitations are small enough, the nonlinear operation of the device can be linearised at the operating point. Such an operation can be modeled by an equivalent circuit called small signal model [10]. It consists of linear elements like resistors, transconductors, capacitors, etc., to represent the small signal currents and charges in the device. In this work pHEMT model is used due to its special features like pHEMTs offer smaller bias sensitivity of noise performance than MESFETs, power back off, better linearity performance, high gain up to millimeter-wavelengths, good noise and power performance and good reliability characteristics[7].

II. COLLECTIVE RESEARCH BACKGROUND

In this section few researches have presented. O.J. Xian, N. Ahmad, M. Mohamad Isa, Siti S. Mat Isa, Muhammad M. Ramli, N. Khalid, N.I. M. Nor, S.R.Kasjoo and M. Missous.et.al, [7] in this work, InGaAs/InAlAs/InP pHEMT sample #XMBE141 is used. Under this group of pHEMT, there are three transistors with different gate width have been selected to model. They are 4 x 75 µm, 4 x 100 µm and 4 x 200 µm with 1 V 10%, 1 V 20%, 1.5 V 10% and 1.5 V 20% biasing. Therefore, there is a total number of twelve small signal models are modeled. The frequency range of interest is from 200 MHz to 10 GHz. Shakti Tripathi, Gurjit Kaur. et.al, [8] presents the values of s-parameters show that the impedance matching of the network is done successfully. The GaN HEMT exhibits fine operation in the frequency range of 1 GHz to 50 GHz. The values of noise figure and noise factor suggest that the transistor is highly immune to noise in the selected frequency range. D.Resca, A.Santarelli, A.Raffo, R.Cignani, G.Vannini, F.Filicori. et.al, [9] described that EM based identification of distributed parasitic leads to an intrinsic device which is physically consistent and can be accurately described by using a conventional equivalent circuit model. Z. Hemaizia, N. Sengouga& M. Missous. et.al, [2] this work presented a direct extraction method of the elements of small signal equivalent circuit of two transistors PHEMT one on the GaAs substrate and the other on the InP substrate of which the length and the width of the gate respectively 1µm and 200 µm. This modeling is essential for any active or passive component and which precedes any design of a radio frequency circuit. Andreas R. Alt, Diego Marti, and C.R.

Bolognesi.et.al, [10] in this work, a detailed review of the HEMT SSEC (small signal equivalent circuit) models was given. A new extrinsic SSEC was then introduced to properly describe pad capacitances on various substrates and buffer materials, regardless of their residual conductivity.

III. METHODOLOGY

In this section proposed model block diagram and equivalent circuit of proposed model and conventional transistor with their descriptions are shown. Fig. 1 shows the overall flow of small signal modeling process of pHEMT based transistor. Overall, there are five steps to be performed in this small signal modeling process.

A. Proposed model

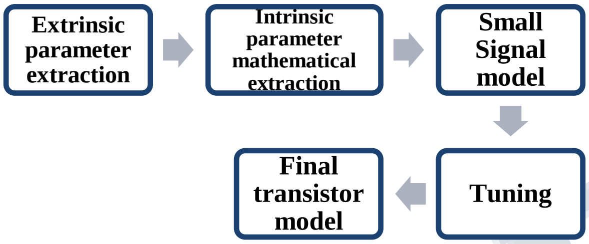


Fig. 1 Overview of small signal modeling of pHEMT based transistor

B. Model description

There is a network of lumped elements as extrinsic circuit, in which capacitor and inductor are connected in series to a gate terminal, a capacitor to a drain terminal and source is grounded. Similarly, there is an intrinsic element network where the topology of small-signal model for AlGaN/GaN HEMTs is shown in fig 3. The main nonlinear elements of the model consist of the nonlinear drain-source current Ids, the gate-source capacitor Cgs, and the gate-drain capacitor Cgd. The gate-source and gate-drain diode characteristics are modeled using the Schottky ideal diode, equation (19) [18].The parameters of the diodes were extracted from forward bias IV measurements (not to damage the gate terminal due to excessive forward current).

$$\mathrm{I_D = I_s(e^{\frac{VD}{nVT}} - 1)}. \qquad (19)$$

C. Mathematical Modeling

I/V Characteristic:

$$Id = Ipk.AFAC.(1+\tanh(\Psi))(1+\lambda.Vd)\tanh(\alpha.Vd) \qquad (1)$$

Where, $\Psi = \mathrm{P1.Vgf + P2.Vgf^2 + P3.Vgf^3}$ (2)

Breakdown is modeled by modifying Vg as follows:

$$\mathrm{Vgr = Vg + B1(Vd - Vdb) + B2(Vd - Vdb)^2 - Vpk} \qquad (3)$$

The B1 and B2 terms are not in the original model. They promote a simpler expression for soft breakdown [13].

Capacitances:

$$\mathrm{Cgs = AFAC.CGS0(1 + \tanh(\varphi 1))(1 + \tanh(\varphi 2))} \qquad (4)$$

Where,

$$\mathrm{\varphi 1 = P10 + P11.Vg} \qquad (5)$$

$$\mathrm{\varphi 2 = P20 + P21.Vdg} \qquad (6)$$

$$\mathrm{Cgd = AFAC.CGD0(1 + \tanh(\varphi 3))(1 - P400.\tanh(\varphi 4))} \qquad (7)$$

Where,

$$\mathrm{\varphi 3 = P30 + P31.Vg} \qquad (8)$$

$$\mathrm{\varphi 4 = P40 + P41.Vdg} \qquad (9)$$

Charge Function:

$$\mathrm{Qgs = AFAC.CGS0(1 + \tanh(\varphi 2))[Vg + \frac{1}{P11}\log(\cosh(\varphi 1))]} \qquad (10)$$

$$\mathrm{Qgd = AFAC.CGD0(1 + \tanh(\varphi 3))[Vdg\text{-}\frac{P400}{P41}\log(\cosh(\varphi 4))]} \qquad (11)$$

Gate-to-drain and gate-to-source diodes are modeled by PNIV (diode junction) elements.

Parameter Scaling:

$$\mathrm{RGG = \frac{RG.AFAC}{NFING^2}} \qquad (12)$$

$$\mathrm{RDD = \frac{RD}{AFAC}} \qquad (13)$$

$$\mathrm{RSS = \frac{Rs}{AFAC}} \qquad (14)$$

$$\mathrm{RII = \frac{RI}{AFAC}} \qquad (15)$$

$$\mathrm{RDSFF = \frac{RDSF}{AFAC}} \qquad (16)$$

$$\mathrm{CDSS = CDS.AFAC} \qquad (17)$$

$$\mathrm{CDSFF = CDSF.AFAC} \qquad (18)$$

Input impedance:

$$\mathrm{Z_{in} = Z_L + Z_C = j(X_L + X_C) = j(wL - \frac{1}{wC})} \qquad (19)$$

Output impedance:

$$\mathrm{Z_0 = j\frac{1}{XC}}$$

(20)

VSWR: (Voltage standing wave ratio)

$$\mathrm{\Gamma = \frac{(Z_L - Z_0)}{(Z_L + Z_0)} = VSWR = \frac{(1 + |\Gamma|)}{(1 - |\Gamma|)} = \frac{(1 + |S11|)}{(1 - |S11|)}} \text{ at input port}$$

$$\mathrm{\frac{(1 + |S22|)}{(1 - |S22|)}} \text{ At output port} \qquad (21)$$

$$\mathrm{G = |S21|} \qquad (2$$

Where,

P1, P2, P3= I/V polynomial coefficient

B1, B2= Soft breakdown polynomial coefficient
VdB =Sub threshold voltage parameter
Vpk=Gate voltage at peak Gm
Alpha (α) =Drain I/V knee parameter
(λ) =Drain-source resistance parameter
Ipk= Current at peak Gm (50mA)
CGS0 =Gate-source capacitance parameter
P10, P11, P20, P21= Gate-source capacitance polynomial coef.
Cgd =Gate-drain capacitance parameter
P30, P31, P40, P41, P400= Gate-drain capacitance polynomial coef.
AFAC=Gate width scale factor
NFING=Number of fingers scale factor
CDSF=Capacitance that determines Rds break frequency
RDSF=RF drain-source resistance
r= Reflection coefficient
S11= Input port voltage reflection coefficient
S12=Reverse voltage gain
S21=Forward voltage gain
S22=Output port voltage reflection coefficient

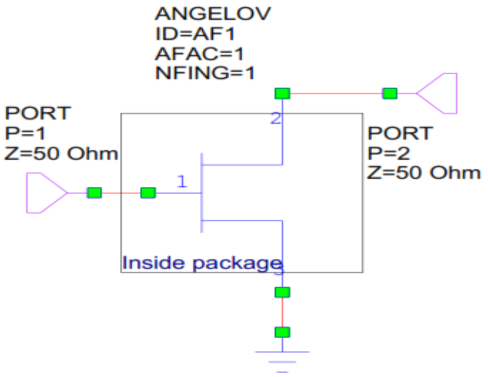


Fig.2 Conventional transistor model without extrinsic element

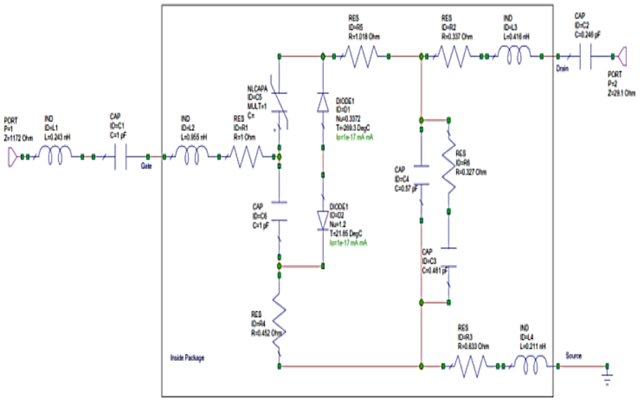
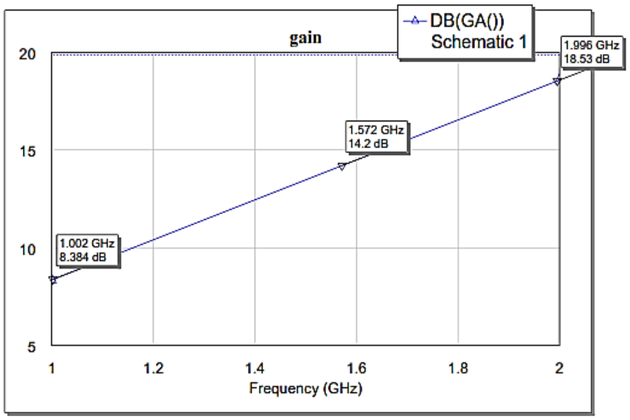


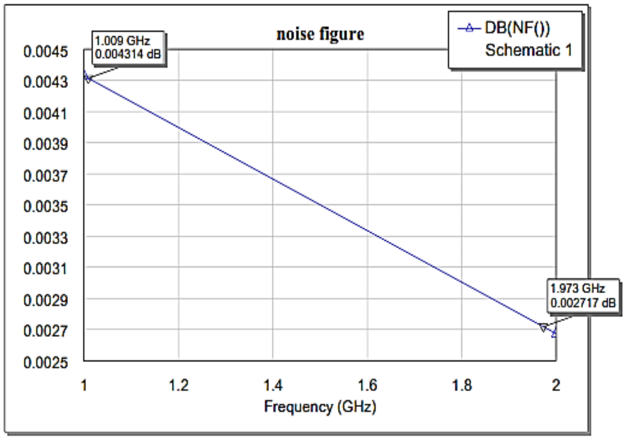
Fig.3 Proposed Model

IV. RESULT

In this section, four major measurements such as Gain, Stability, and S-parameter and Noise figure of a transistor have shown graphically.



(a)



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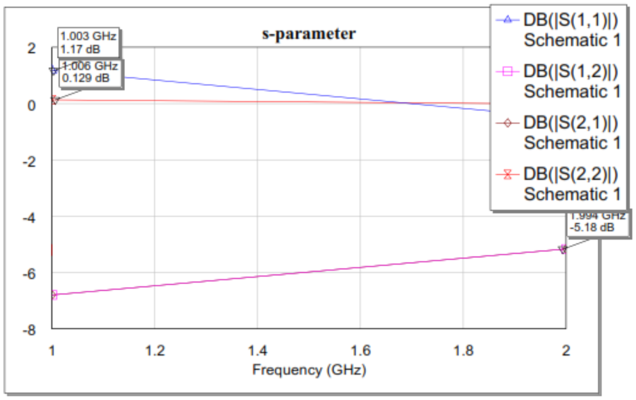

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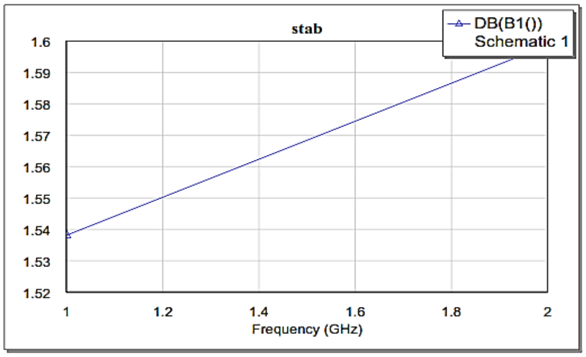
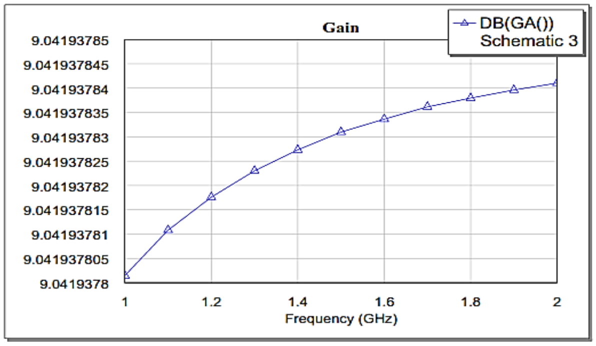
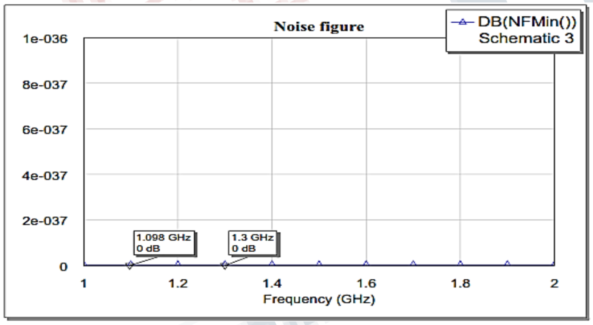


(d)

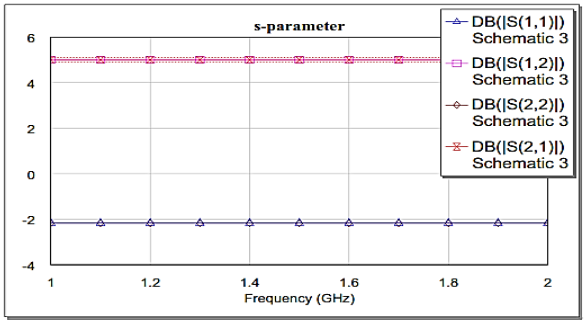
Fig 4: (a) Gain, (b) NF(Noise figure), (c) S-parameters, (d) Stability of proposed model in dB at 1-2GHz



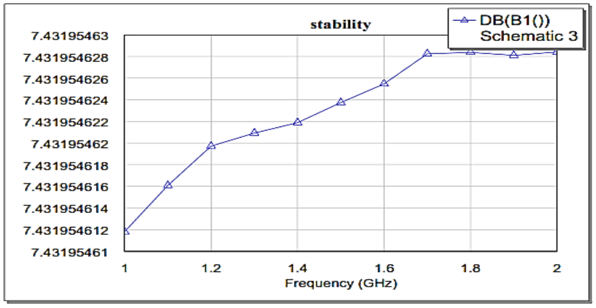
(a)



(b)



(c)



(d)

Fig 5: (a) Gain, (b) NF(Noise figure), (c) S-parameters, (d) Stability of conventional model in dB at 1-2GHz

Below is the table of comparison between proposed model and conventional model on the basis of Gain and stability. This comparison shows the proposed model a better transistor design with respect to Gain measurement.

Table 1. Comparison between measurements of proposed model and conventional model

Parameters	@1-2GHz (dB) Proposed model	@1-2GHz(dB) Conventional model
Gain	8.384 - 18.53	9.0419
Stability	1.54 - 1.6	7.4319

The fig.4 shows the experimental values of Gain, Stability, Noise figure and S-parameters, where Gain is 18.53 dB at 2GHz that is it is increasing with frequency. For a good transistor Gain should be high. Noise figure is minimum for 2 GHz frequency; it should have minimum value for better transistor functioning. For good S-parameter (Scattering parameters) data the following conditions must be satisfied: - For passive reciprocal parts, S12 must equal S21. For passive parts, S12 and S21 can't be greater than 0 dB, where the parameters S11, S22 have the meaning of reflection coefficients, and S21, S12, the meaning of transmission coefficients. These conditions are satisfying with proposed model circuit at 2 GHz frequency. At microwave frequency stability of a transistor should be near to unity, in this work the value of stability is near to unity which is satisfactory at 2GHz frequency with the proposed model. The performance of a good transistor depends on S21 parameter which leads to high complex linear gain and scalar linear gain, equation (22). A higher ratio of VSWR, equation (21) depicts a larger mismatch, while 1:1 ratio is perfectly matched. This match or mismatch arises from the standing wave's maximum and minimum amplitude. Now, the fig.5 shows the gain of 9.0419dB at 1-2GHz frequency which is less than gain of the proposed model.

V. CONCLUSION AND FUTURE WORK

An equivalent circuit transistor device demonstrates in the light of a simulation and mathematical portrayal of extrinsic and intrinsic components. An established comparable equivalent circuit small-signal model has been extracted starting from a linear parasitic network. The outcomes demonstrate gain, noise figure, s-parameter and stability of a transistor model. The intrinsic device which is precisely portrayed by utilizing a conventional equivalent circuit model. The better fitting of the intrinsic device and the good scaling properties with respect to an equivalent circuit model based on lumped elements have been illustrated. The future work will be to estimate better results and mathematical analysis in terms of linear and nonlinear parameters. In contrast with the proposed model, industrial models will be focusing on the projection of transistor fabrication.

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REFERENCES

1. Bowman, M., Debray, S. K., and Peterson, L. L. 1993. Reasoning about naming systems. .
2. J. Schleeh, G. Alestig, J. Halonen, A. Malmros, B. Nilsson, P. A. Nilsson, J. P. Starski, N. Wadefalk, H. Zirath, and J. Grahn, “Ultralow-power cryogenic InP HEMT with minimum noise temperature of 1 K at 6 GHz,” IEEE Electron Device Lett., vol. 33, no. 5, pp. 664–666, May 2012.
3. Z. Hemaizia, N. Sengouga& M. Missous,” SMALL-SIGNAL MODELING OF PHEMTS AND ANALYSIS OF THEIR MICROWAVE PERFORMANCE”, Université Mohamed Khider – Biskra, Algérie, 2010.
4. Joel Schleeh, NiklasWadefalk, Per-Åke Nilsson, J. Piotr Starski, Senior Member, IEEE, and Jan Grahn, Senior Member, IEEE,” Cryogenic Broadband Ultra-Low-Noise MMIC LNAs for Radio Astronomy Applications”, IEEE transactions on microwave theory and techniques, vol.61,no.2, february2013.
5. J.Schleeh, H.Rodilla, N.Wadefalk, P.A.Nilsson, andJ.Grahn,“Characterization and modeling of cryogenic ultra-low noise InP HEMT,” IEEE Trans. Electron Devices, 2013, to be published.
6. Angel Mediavilla, Tomás Fernandez, J.A. García Antonio Tazón, F. Marante,”Equivalent Circuit MESFET/HEMT Modeling Approaches”Dpto. Telecomunicaciones –ISPJAE-La Habana.
7. J. Schleeh, G. Alestig, J. Halonen, A. Malmros, B. Nilsson, P. A. Nilsson, J. P. Starski, N. Wadefalk, H. Zirath, and J. Grahn, “Ultralow-power cryogenic InP HEMT with minimum noise temperature of 1 K at 6 GHz,” IEEE Electron Device Lett., vol. 33, no. 5, pp. 664–666, May 2012.
8. O.J. Xian, N. Ahmad, M. Mohamad Isa , Siti S. Mat Isa, Muhammad M. Ramli, N. Khalid, N.I. M. Nor, S.R.Kasjooand M. Missous,” Small Signal Modeling of Novel InGaAs/InAlAs/InP pHEMT for High Frequency Applications”, 2016 3rd International Conference on Electronic Design (ICED), August 11-12, 2016, Phuket, Thailand.
9. Shakti Tripathi,Gurjit Kaur, PhD School of ICT,” Analysis of Noise Figure of GaN HEMT at High Frequency Range for Microwave Applications”,International Journal of Computer Applications (0975 – 8887)Volume 70– No.20, May 2013.
10. Kishor G. Sawarkar, Pramod K.B, Kushal Tuckley, KumaraswamyH.V,” A Design and Analysis of Noise Figure Optimization of aWideband PHEMT Hybrid LNA with Flat Gain for WiMAX Application”, International Conference on Computer Technology (ICCT 2015).
11. D.Resca, A.Santarelli, A.Raffo, R.Cignani, G.Vannini, F.Filicori,“Scalable Equivalent Circuit PHEMT modeling usingan EM-based parasitic network description,” Proceedings of the 2nd European Microwave Integrated Circuits Conference, October 2007.

12. Andreas R. Alt, Diego Marti, and C.R. Bolognesi, “Transistor modeling,” IEEE microwave magazine, June 2013.

13. Angelov, "Chalmers Nonlinear HEMT and MESFET Model Extraction Procedure, Part A," Chalmers University of Technology, Dept. of Microwave Technology, Report no. 25, July, 1996.

14. Angelov, "Chalmers Nonlinear HEMT and MESFET Model Extraction Procedure,Part B," Chalmers University of Technology, Dept. of Microwave Technology, Report no.26, November, 1996.

15. Angel Mediavilla, Tomás Fernandez, J.A. García Antonio Tazón, F. Marante,”Equivalent Circuit MESFET/HEMT Modeling Approaches”Dpto. Telecomunicaciones –ISPJAE-La Habana.

16. T R Lenka & A K Panda,” Effect of structural parameters on 2DEG density and C-V characteristics of$Al_x\, Ga_{1-x}\ N/AIN/\ GaN$ based HEMT”, National Institute of Science and Technology (NIST), Berhampur, Odisha 761008,India, Indial Journal of Pure & Applied Physics,vol.49,June 2011,pp.416-422.

17. Francesco Fornetti,” Characterisation and Performance Optimisation of GaNHEMTs and Amplifiers for Radar Applications”, December 2010.

18. Zhang Wen,Yuehang Xu, Changsi Wang,Xiaodong Zhao, Zhikai Chen and Ruimin Xu,” A parameter extraction method for GaN HEMT empirical large signal model including self-heating and trapping effects”, 21 December 2015 in Wiley Online.